

### REMARKS

Claims 1, 8-18, and 23-25 are pending in the application. Applicants note with appreciation the allowance of claims 13-18 and 23-25. Reconsideration of the application in light of the following remarks is respectfully requested.

#### I. REJECTION OF CLAIMS 1 AND 8-12 UNDER 35 U.S.C. § 103(a)

Claims 1 and 8-12 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent Application Publication No. 2004/0120339 (Ronciak) in view of U.S. Patent Publication No. 7,003,647 (Jacobs et al.). Withdrawal of this rejection is requested for at least the following reasons.

##### *i. The cited art does not teach or suggest assembling a coalesced array from a coalesced physical buffer, as provided in claim 1.*

Independent claim 1 recites a method for partially coalescing transmit buffers, comprising assembling a coalesced array from a coalesced physical buffer and one or more respective non-selected and non-coalesced virtual or physical buffers. The Office Action concedes that Ronciak fails to teach this aspect of the present invention, but instead relies upon Jacobs et al. to teach a coalesced array that is assembled from a coalesced physical buffer and one or more respective non-selected and non-coalesced virtual or physical buffers. (See, O.A. of 1/5/10, p. 3, Ins. 8-16). However, as will be more fully appreciated below, Jacobs et al. fail to teach **a coalesced array that is assembled from a coalesced physical buffer**, as recited in claim 1.

In particular, Figs. 5A-5C and 6A-6B illustrate a preferred embodiment of a method for coalescing page table entries (PTEs), comprising an iterative mapping of PTE virtual addresses to PTE physical addresses. As shown in Fig. 5A, pages that can be coalesced are determined by looking at, inter alia, page sizes and a start\_pte address. (See, e.g., Fig. 5A, actions 506 and 510). For pages that can be coalesced, a PTE virtual address (part of initial state 602) is mapped. Once a mapping is complete, the virtual address is incremented (e.g., at 528) and the mapping process is repeated to

include additional PTE virtual addresses.

For example, as shown in Figs. 6A-6B, a first loop would (e.g., having a NATURAL\_BLOCK\_SIZE\_MULTIPLIER = 4) have start\_pte with vaddr 00048000 and would map PTEs referencing virtual addresses 00049000, 0004A000, and 0004B000. A subsequent loop would have start\_pte with vaddr 00040000 and “would map [PTEs referencing] virtual addresses 00044000, 00048000, 0004C000.” (See, col. 11, Ins. 20-33)(emphasis added). Therefore, Jacobs et al. teach a method for assembling a PTE physical address using subsequent loops that respectively map PTE virtual addresses to form a PTE physical address.

In contrast, claim 1 recites a method for coalescing comprising assembling a coalesced array *from a coalesced physical buffer*. However, as taught by Jacobs et al., *each subsequent loop used to assemble a PTE physical address references virtual addresses*. (See, col. 11, Ins. 20-33 and Ins. 63-65). Since Jacobs et al. teach that subsequent loops used to assemble a PTE physical address are mapped from PTE's referencing virtual addresses, Jacobs et al. do not teach forming a coalesced array *from a coalesced physical buffer*. Accordingly, withdrawal of the rejection of independent claim 1 and the rejected claims depending thereupon is respectfully requested.

**II. CONCLUSION**

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP772US.

Respectfully submitted,  
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